Problem C: GPU Accelerated Logic Rewriting
Ghasem Pasandi, Sreedhar Pratty, David Brown
NVIDIA Corp., Santa Clara, CA

Q&A

Q1. In the evaluation part, the script are scored based on the run-time and GPU utility. Any requirement about QoR of the output circuit of our implementation? Are we allowed to change the methodology of rewrite (e.g. change the traversal order, cut enumeration algorithms, ...), which will probably result in a different QoR?
A1. AIG node count is added to scoring function as QoR, and in the new revision of the problem, changes like traversal order, cut enumeration algorithms are allowed.

Q2. It it possible to implement the "standard" rewriting algorithm as the one in ABC and innovate with respect to the algorithmic design? Is the rewriting quality (in terms of circuit size reduction) evaluated? Currently, it is not involved in the scoring function, which means one could implement something fast but useless and win the competition.
A2. Please see the revised problem contest. Algorithmic changes are allowed and now there is a QoR metric in the scoring function.

Q3. Is there any space for optimization by using GPU acceleration? how many nodes does the Biggest case has in the benchmarks? I have tested the EFPL benchmarks on the competition website. And I choose the AIG case with the largest area, which has over 200 thousand "AND nodes". But it only costs about three seconds to run "drw" in abc. I'd like to know if there is any space for optimization by using GPU acceleration? And, by the way, may I know how many nodes does the biggest case has in the benchmarks? I've tried to rewrite some functions in a "CUDA" way, but it seems that the effect is not good, and the running time is much longer than before. I think it's because the cuda kernel function has been executed too many times as the case hasmany "AND nodes".
A3. There are larger benchmarks that take much more time than 3 seconds. Take a look at MtM benchmarks: https://www.epfl.ch/labs/lsi/page-102566-en-html/benchmarks/ For sixteen benchmark circuit above, it took ~425 seconds for drw to finish on my system. A good implementation of drw on GPU should be able to decrease this large run-time.

Q4. Please help to advise if we need to support the option paremeter "-C -N -l -f -z -r -v -w -h" in origin "drw" command.
A4. In the final submission, they should support these options but for alpha submission, it is not needed to support them all and a default setting for options should be enough.

Q5. Please help advise if we need to support AIG files with latches.
A5. No, we will test their codes using only combinational circuits.
Q6. Q1. Could we ignore ABC and develop something new that can do the logic rewriting (which could be more GPU-friendly)?

A6. Yes it is okay to bypass ABC and develop a new rewriting function that is GPU-friendly, but the code should support the commands that are required and mentioned in the contest problem such as reading/writing AIGs, etc.

Q7. Could you please help to advise any alternative links of MtM benchmarks? because we cannot download the MtM benchmarks at https://www.epfl.ch/labs/lsi/page-102566-en-html/benchmarks/. We tried to use different networks but they didn't work.

A7. Try this link: https://zenodo.org/record/2572934#.XGxRiS3MzuM