Problem A: X-value Equivalence Checking

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Q&A

Q1. Are input, output and wire in the input file (golden. v and revised. v) only one line or more than one line?

A1. May be multiple lines.

Q2. Is each testcase only one output signal? If there are many output signal, I should check all output and write one answer or one answer for one output?

A2. Multiple outputs signals. One EQ/NEQ as the answer. NEQ if there is any output NEQ, otherwise EQ.

Q3. 1.If the wire is more than one line, which format of input file is it?

wire a, b, c, d, or wire a, b, c, d;
e, f, g; wire e, f, g;

2. n the 3.4 example of problem A, the expected output is
NEQ
in 1
a 1
b 0

However, there is another witness like
NEQ
in 0
a 1
b 0

Is it correct if there are many witness and I just output an arbitrary correct witness?

For instance, in 3.4 example, and my output is
NEQ
in 0
a 1
b 0

A3. Both are possible. Yes, arbitrary witness are okay.

Q4. AND, XOR, OR only have two inputs and one output, is right?

A4. Primitive gates (and, or, nand, nor, xor, xnor) will have multiple inputs (>=2) and single output in Verilog format.
Primitive gates (not, buf) have only one input and one output in Verilog format.

For example: nand inst_name(o1, in1, in2 ,in3 ,…).

Q5. Can you provide some test examples?

A5. Yes, we will provide testcase soon.

Q6. Does the circuit contain loops?

A6. No, the circuits are all combinational circuit without loop.

Q7. Can we use the package, such as CUDD, that can be found online to solve this problem, or we can only solve this problem from scratch?

A7. Yes, no problem. Please make sure you pack library well and program can be executed in testing/evaluation machines.