ICCAD 2018 CAD Contest

Timing-Aware Fill Insertion

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- 2018-08-22- Beta Results announced.
- 2018-08-22- Problem C FAQ is updated

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- 2018-07-31- New checker released: https://github.com/boyangeda/iccad2018-contest
- 2018-07-31- Problem C FAQ is updated
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- 2018-07-05- Problem C FAQ is updated
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Synopsys Inc.

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Introduction

It is a mandatory step in modern semiconductor manufacturing process to fill the empty conductor layers with metal fills, and it is commonly performed after the physical design stage. These fills can reduce the dielectric thickness variation, increase planarity, and provide better pattern density, all of which are important to mitigate the process variability thereby achieving better yield.

Problem Description

When a fill is inserted, it improves the metal density and increases planarity. But on the other hand it inevitably couples to the signal tracks (Figure 1). If the coupling capacitance to a critical net is significant, the original timing-closure may not be achieved anymore. Therefore it is important to reduce the capacitance impact during metal fill insertion.

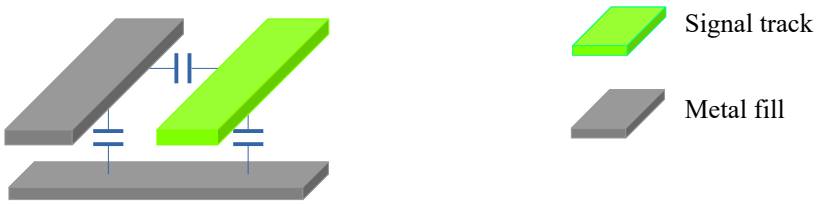


Figure 1: Signal track-metal fill coupling

The current mainstream solution is to set up a keepout region (space around a metal track to its nearest fill, Figure 2) for metal fill around critical signal tracks so that the coupling capacitance introduced by the metal fills can be safely ignored. However, achieving optimum metal fill insertion with this method is a challenge. A large keepout distance could result in sub-optimal metal density and uneven fill patterns that negatively impact yield. Conversely, a small keepout distance could significantly increase capacitance and break timing. Furthermore, the impact on timing is not known without running a parasitic extraction tool. Hence an efficient algorithm to insert optimum metal fill is required.

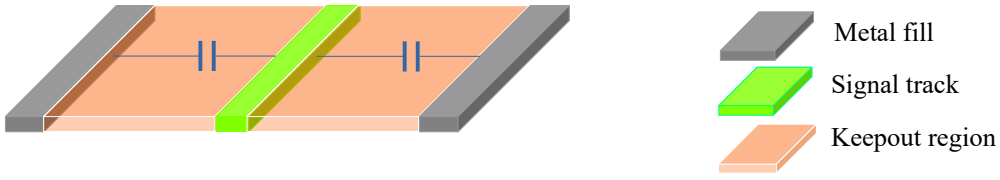


Figure 2: Keepout regions

Capacitance Calculation

The metal fill insertion algorithm needs to account for the impact of capacitance on the signal nets. There are three main types of capacitances that need to be considered when evaluating the impact of metal fill. They are as follows:

1) Area Capacitance

Two conductor pieces will form an area capacitance when a) they are on different metal layers, b) their projections on the ground plane overlap, and c) no other intermediate-layer metal appears between the two conductors in the overlapped region (Figure 3).

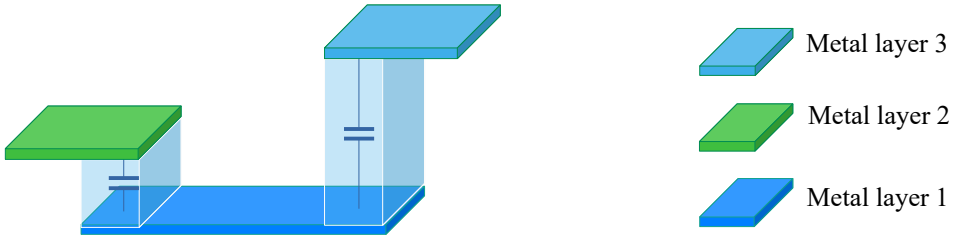


Figure 3: Area Capacitance

For an overlapped area s formed by conductors on layers l_1 and l_2, the area capacitance C_a is calculated by $C_a = P_{l_1,l_2}(s) \times s$, where $P_{l_1,l_2}(s)$ is the area capacitance per unit area and it is a function of overlapped area s.

2) Lateral Capacitance

The lateral capacitance is formed by the conductors on the same layer. Any two conductors that horizontally overlap will form lateral capacitance as shown in Figure 4. The capacitance is calculated by $C_l = P_l(d) \times l$, where l is the length of the parallel edges of the conductors and $P_l(d)$ is the lateral capacitance per unit length, which is a function of distance of the parallel edges d.

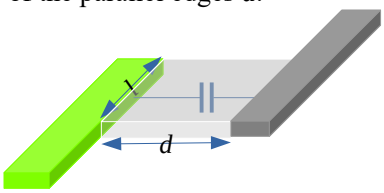


Figure 4: Lateral Capacitance

3) Fringe Capacitance

The fringe capacitance is formed by two conductors on different layers and its calculation is based on the following formula, where these two conductors don't overlap with each other.

$$C_f = \begin{cases} p_{l_1,l_2}(d) \times l + p_{l_2,l_1}(d) \times l, & d \geq 0 \\ 0, & d < 0 \end{cases}$$

where l is the length of parallel edges and d is the horizontal distance of two conductors (Figure 5). d will be negative if the conductors overlap (i.e., $C_a > 0$). $P_{l_1,l_2}(d)$ and $P_{l_2,l_1}(d)$ are the fringe capacitance per unit length.

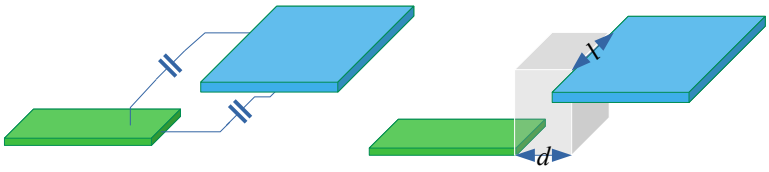


Figure 5: Fringe Capacitance

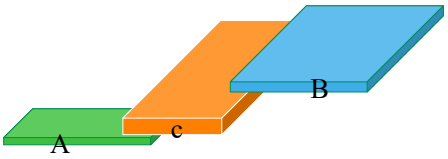


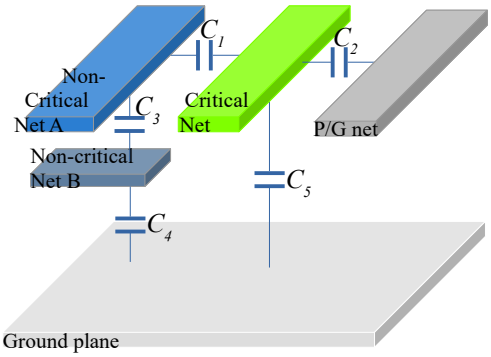
Figure 6: Shielding effect

3.1) Shielding Effect

If two conductors A, B are on the different layers l_1 and l_2, respectively, the fringe coupling between A and B is shielded and the capacitance goes to zero when there is a horizontal conductor on the intermediate layer between A and B. Note that the coupling capacitance to the shielding conductor C still needs to be calculated (Figure 6). In Figure 6, the fringe capacitance between A and B is shielded by C, but the coupling capacitance (either fringe capacitance or area capacitance) between (A,C) and (B,C) need to be calculated.

Total Capacitance Calculation

After metal fill insertion, the total capacitance of a critical net needs to be calculated as the equivalent capacitance to ground. Note that resistance is ignored. All non-critical nets, except for the power/ground nets, are treated as floating. Coupling to the power/ground nets is calculated as direct-coupling to ground (Figure 7).



$$C_{total} = C_2 + C_5 + \frac{C_1 \times C_3 \times C_4}{C_1 \times C_3 + C_3 \times C_4 + C_1 \times C_4}$$

Figure 7: Total capacitance calculation

Metal Density

The layout with metal fill must meet the density criteria. The density is calculated in a window based manner (Figure 8):

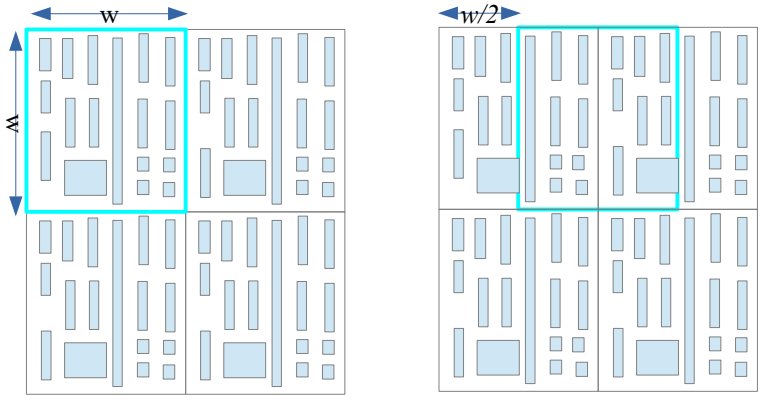


Figure 8: Density Calculation Window

w is the window size for density calculation, and the step length is set to $w/2$. The density in a window W_i is calculated as

$$D_{l,W_i} = \sum_{S \in W_i} S/w^2,$$

where l is the metal layer, and S is the metal area that is enclosed inside W_i. The density in each window must be larger than the given metal density for that layer.

Algorithm Evaluation

The optimization algorithm should insert metal fills subject to the density criteria and design rules, while minimizing the total capacitance of a given critical net. Metal fills must not introduce any design rule violation. Results with design rule violation will not be accepted for further evaluation. Results need to pass the window-based density check. Results with density violation will be rejected as well.

The accepted result with smaller total capacitance will get higher quality score with the highest of 15 points. For instance, the best result (smallest total cap) gets 15 points and the second place gets 14 points. The accepted result with shorter run time gets higher performance score with the highest of 5 points. For instance, the result with shortest run time gets 5 points and the second place gets 4 points. Results beyond the the fifth place in run time do not get any performance points.

Teams will be ranked by the sum of quality points and performance points.

Benchmark suites

Five benchmark cases will be provided along with one rule file and one process file which describe design rules and process-related information. The benchmark cases are all text files with different number of polygons (rectangular). Lines starting with a semicolon (;) are comments.

Layout File Format:

```
; The first non-comment line of layout file is the chip boundary:
;   bottom_left_x bottom_left_y top_right_x top_right_y
Chip_boundary_BL_x Chip_boundary_BL_y Chip_boundary_TR_x Chip_boundary_TR_y

; Polygon_id is a positive integer. The polygon type will be one of the four types:
; Drv_Pin that marks this polygon is a drive pin of the net,
; Normal marks this polygon is a normal conductor,
; Load_Pin indicates the polygon is a load pin, and
; Fill indicates this is a fill polygon.

; For a fill polygon, its net id can be set to any integer.
Polygon_id bl_pt tr_pt net_id layer_id <polygon type: Drv_Pin|Normal|Load_Pin|Fill>
```

Rule file:

```
Layer_id <conductor|via> min_width min_space max_fill_width min_density max_density
```

Please note that the density criteria does not apply to via layer, so if the second field of the rule file is `via`, `min_density` will be set to `0` and max_density will be `1`.

Process file:

```
; Window size for density calculation (unit: nanometers)
window: 5000

; Unit Capacitance
; when a table does not exist, it’s marked by ‘*’
; lateral_table_* can be thought of as a special case of fringe_table_*
; layer id (layer id 0 is ground plane)
```

	1	2	...	n
0	(area_table_1_0,*)	(area_table_2_0, *)		(area_table_n_0, *)
1	(*, lateral_table_1)	(area_table_1_2, fringe_table_1_2)	...	(area_table_1_n, fringe_table_1_n)
2	(area_table_2_1, fringe_table_2_1)	(*, lateral_table_1)	...	(area_table_2_n, *)
...	...	...	...	...
n	(area_table_n_1, fringe_table_n_1)	(area_table_n_2, fringe_table_n_2)	...	(*, lateral_table_n)

```
TableName: area_table_1_0
; p(s)= a*s + b
; the unit cap is a piece-wise linear function of s
;  s1=<s <s2, s2=<s<= s3 …
s1,  s2, s3, ...
(a1, b1), (a2, b2), (a3, b3) ….

TableName: area_table_1_2
; p(s)= a*s + b
; the unit cap is a piece-wise linear function of s
;  s1=<s <s2, s2=<s< s3 …
s1,  s2, s3, ...
(a1, b1), (a2, b2), (a3, b3) ….

TableName: area_table_1_3
; p(s)= a*s + b
;
s1, s2, s3, ...
(a1, b1), (a2, b2), (a3, b3) ….
...
...
; lateral cap table
TableName: lateral_table _1
; p(d) = a*d + b
d1, d2, d3, …
(a1, b1), (a2, b2), (a3, b3)…
...
; fringe cap table
TableName: fringe_table_1_0
; p(d) = a*d +b
d1, d2, d3, …
(a1, b1), (a2, b2), (a3, b3)…
```

The contest program should read in an config file, for example, input.conf, to parse all necessary files and parameters:

```
; Test1
design: <benchmark_file_name>
output: <output file>
rule_file: <design rule file>
process_file: <process file>
critical_net: net_id1, net_id2,...
power_nets: power_net1, power_net2, …
ground_nets: ground_net1, ground_net2, …
```

The program should output a design with metal-fills. The output file format should be same as input benchmark file.

Cap Extraction Example

Example1.conf:

```
design: example1.layout
output: example1.fill
rule_file: rule.dat
process_file: process.dat
critical_net: 1
power_nets: 2
ground_nets: 0
```

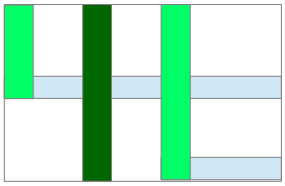


Figure 9: Example layout with one metal-fill (dark green rectangle)

Example1.layout:

```
0 0 100 80 ; chip boundary
1 60 0 100 10 2 1 Normal; A normal polygon on layer 1 (net 2: power)
2 0 40 100 50 1 1 Normal; A normal polygon on layer 1 (net 1: critical net)
3 0 40 10 80 1 2 Normal; A normal polygon on layer 2 (net 1: critical net)
4 60 0 70 80 2 2 Normal; A normal polygon on layer 2 (net 2: power)
```

rule.dat:

```
;Layer_id <conductor|via> min_width min_space max_fill_width min_density max_density
1 conductor 10 10 30 0.3 1
2 conductor 10 10 30 0.3 1
```

process.dat:

```
;table matrix, layer id 0 means ground plane
        1                           2
0 (area_1_0, *)          (area_2_0, *)
1 (*, lateral_1)         (area_2_1, fringe_2_1)
2 (area_2_1, fringe_1_2) (*, lateral_2)
; process tables
TableName: area_1_0
  100                 200            300   400
  (0.01, 0.017) (0.0102, -0.02) (0.0101, 0.015)

TableName: lateral_1
  10                 50         100       200
  (0.01, 0.017) (0.0102, 0.001) (0.0101, 0.015)

TableName: fringe_1_2
  0                  50          100       150
  (0.007, 0.012) (0.0102, 0.001) (0.0101, 0.015)


TableName: area_2_0
  100                 150         200       300
  (0.01, 0.017) (0.0102, -0.01) (0.0101, 0.015)

TableName: area_2_1
  100                 300         400      500
  (0.01, 0.017) (0.0102, -0.02) (0.00101, 0.015)

TableName: lateral_2
  10                 50          100    200
  (0.01, 0.011) (0.0102, 0.001) (0.0101, 0.015)

TableName: fringe_2_1
  10                 50         100       150
  (0.011, 0.01) (0.0102, 0.001) (0.0101, 0.015
```

Now assuming the metal-fill output file example1.fill:

```
1 30 0 40 80 0 2 Fill; A metal-fill on layer 2
```

The coupling capacitance between the critical net (net id 1) and the metal-fill consists of 1) area-capacitance between polygon 2 and the fill polygon, and 2) lateral-capacitance between polygon 3 and the fill.

For the area capacitance, the overlapped area is 100 nm^2 between layers 1 and 2. Hence the area cap table should be `area_2_1`. Since the area is between index 100 and 300, the coefficients 0.01 and 0.017 are selected to calculate the unit area capacitance:

C_{unit} =0.01x overlapped area + 0.017 = 1.017 ff/nm^2 ,

and the area-capacitance is

C_{unit} x overlapped area = 101.7ff.

Please note that if the overlapped area is larger than the largest area sampling point of the area cap table, then the largest sampling point is used to calculate an initial capacitance and then scaled by a factor of overlapped-area /

largest area-sampling point. For instance, assuming an overlapped area of 800 nm^2 formed by two polygons on layers 1 and 2, and since the largest sampling point in the table `area_2_1` is 400nm^2, we use 400 to calculate an initial cap:

C_{init} = (0.0101 x 400 + 0.015)x400 = 1622 fF

The final area capacitance is calculated by

$C_{area} = C_{init}$ x (800/400) = 1622 x 2 = 3244 fF

A similar procedure can be applied when the overlapped area is smaller than the smallest area sampling point:

$C_{area} = C_{init} * S_{overlap}/S_{min\_sampling\_area}$,

where C_{init} is the initial capacitance calculated with the smallest area sampling point, $S_{overlap}$ is the overlapped area and $S_{min\_sampling\_area}$ is the smallest sampling point in the table.

For the lateral-capacitance between polygon 3 and the fill polygon, the distance of the two polygons is 20nm, and the table `lateral_2` is used. Since 20nm is between 10nm and 50nm, we choose the first coefficient pair: (0.01, 0.011). Then the unit capacitance will be:

C_l = 0.01 * 20 + 0.011 = 0.211 ff/nm.

Since the parallel edges between the polygons are 40nm long, the lateral-capacitance will be

C_l x 40nm = 8.44 ff

Similar, we can calculate the coupling cap between the fill polygon and net 2 (power net). Note that there is a fringe cap between polygon 1 and the fill polygon. The distance between polygon 1 and the fill is 20nm. Two tables need to considered: `fringe_2_1` and `fringe_1_2` (because metal layers have different thicknesses, the two tables may not be the same). We can get two unit capacitance:

C_{f12} = 0.007 X 20 + 0.012 = 0.152/nm

C_{f21} = 0.011 X 20 + 0.01 = 0.23/nm

The parallel edge length is 10nm, so the fringe capacitance between the file and polygon 1 will be

C_{f12} * 10nm + C_{f12}*10nm = 3.82 ff.

Note that for any lateral-capacitance or fringe-capacitance due polygons with horizontal distance larger than the largest sampling point in the corresponding unit-cap table, the capacitance can be assumed to be zero because the value is small.

Reference

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[2] Y. Chen, P. Gupta and A. B. Kahng, "Performance-Impact Limited Area Fill Synthesis", Proc. ACM/IEEE Design Automation Conf., June 2003, pp. 22-27.

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[6] Kahng, Andrew B and Topaloglu, Rasit Onur, “Performance-aware CMP fill pattern optimization”, in Proc. VMIC, 2007

[7] VS Shilimkar, SG Gaskill, A Weisshaar, “Impact of metal fill on on-chip interconnect performance”, 2009 The 42nd International Symposium on Microelectronics, 983-990

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III. Alpha Test Announcement

The team of top 3 as there were only 3 teams close to run the cases successfully (actually none of them passed both design rule checking and density checking) so it's kind of meaningless to do a complete evaluation.

Beta Test Announcement

Eleven teams provided their executables for the beta evaluation. Four teams (ranked from 1 - 4, marked in green) passed all five test cases and one team passed four tests (ranked 5, marked in blue). All fill files which passed design-rule checking and density checking are extracted for total cap evaluation.

IV. FAQ

Q1. I can't find any info about window size in the file format of benchmark suite, so how can we read in window size info?

A1. new parameter (window) is added into the process file:
window: window size

Q2. In Figure 7, should there have fringe capacitance between critical net and non-critical net B?

A2. This is just an example to explain how to calculate the total capacitance by assuming the couplings are extracted as shown in the figure.

Q3. In III. Algorithm Evaluation, is quality score is measured by the sum of total capacitances of all critical nets in all benchmark cases?

A3. Yes.

Q4. The object is only minimize capacitance effect and runtime described in the Problem Description when doing fill insertion? or other objects like density, etc.

A4. Yes, the object is only to minimize capacitance effect and run-time. The density requirements can be considered as constraints that after filling, density in each window must meet the requirement within given range.

Q5. From Q1, If we need to minimize density, how can we get lower bound and upper bound constraint?

A5. Inside the rule file, each layer has min/max constraints.

Q6. The shape of Insertion Filler is only rectangle? or others like diamond, etc.

A6. Yes, ONLY rectangle are accepted.

Q7. When will you release testcase?

A7. Two cases will be released by 4/23/2018. Other three will be released in May.

Q8. How to calculate parallel capacitance?

A8. Please see II. 2) Lateral Capacitance and the example.

Q9. Can we connect dummy fill to power or ground poly?

A9. No, you cannot as it will pose difficulty for design rule checking. I.e., Fills are not allowed to touch any signals.

Q10. When will you release testcase?

A10.Two cases will be released by 4/23/2018. Other three will be released in May.

Q11. Which density criteria should we satisfy? In "Metal Density" section, the description says "The density is calculated in a window based manner", in other words, we need to satisfy window density constraint. But in "Rule file" section, the description of density constraint is behind layer id. Is this min_density and max_density is the window constraint for every window in this layer? or these constraints are layer constraints (We just need to calculate density for a layer and satisfy these constraints)

A11. The density constraint applies to each layer. In other words, for each layer, we will perform a window-based check.

Q12. What is the table naming rule?

In row layer 0 and column layer 1, the name is area_table_1_0 ->first number is column number and second number is row number. But in row layer n column layer 1, the name is area_table_n_1->first number is row number and second number is column number. Which one is the correct rule?

	1	2	...	n
0	(area_table_1_0,*)	(area_table_2_0, *)		(area_table_n_0, *)
1	(*, lateral_table_1)	(area_table_1_2, fringe_table_1_2)	...	(area_table_1_n, fringe_table_1_n)
2	(area_table_2_1, fringe_table_2_1)	(*, lateral_table_1)	...	(area_table_2_n, *)
...	...	...	...	...
n	(area_table_n_1, fringe_table_n_1)	(area_table_n_2, fringe_table_n_2)	...	(*, lateral_table_n)

A12. There is no rule in naming a table. One should check the name matrix to get the right table name.

Q13. Filler type is 0 in example1.fill, but type 0 is ground nets. Is the type always ground nets when we inserting fill?

```
1 30 0 40 80 0 2 Fill; A metal-fill on layer 2
```

A13. The net id is not used in the fill file, just to main format consistency. All fills are treated as floating (meaning they should not touch any signals).

Q14. Could we insert dummy fill in via layer?
A14. No, only metal fills are allowed.

Q15. The answer of "Could we insert dummy fill in via layer" is yes. No, only metal fills are allowed. We think you may have a misunderstanding. The question we wanted to ask is **Can we insert dummy fill in "VIA Layer"**? (Because we don't need to consider area criteria in this layer, we want to know that inserting in via layer is legal or not?)
A15. To further clear the problem, I've removed all via layers from the rule file and test data. So the answer is still no. But in the real design, via FILL is allowed and the designer is encouraged to fill as many vias as possible to the top via layer, in order to improve yield.
"

Q16. The questions is about testcase file
In "rule.dat", you provide layer 1 to layer 19's constraint
In "Circuit1.cut", there are lots of poly in layer 10-19
But in "process.dat", it only provides us layer 0-9's capacitance table.
How to calculate capacitance when poly in layer 10-19?
A16. All via layers have been removed.

Q17. In "circuit1.cut" line 367, "net id" is 70144. But we can't find net id 70144 in circuit1.conf. Is this a wrong Id? or How to do when we get a non-defined Id?
A17. The nets whose ids are specified in the config file are "critical nets", meaning we should minimize the timing impact to them when inserting metal fills.

Q18. What's the difference if a polygon is Drv_pin or Load_pin compare with Normal or Fill when calculating capacitance?
A18. You can ignore the pin types. Ideally, we should calculate the delay from drv_pin to load_pin in order to more accurately evaluate the timing impact from the metal fills. But this will pose great difficulty. So please ignore them.

Q19. Can we insert FILL into via layer? Do we need to consider the connection between the vias and their upper and lower conductor layer? If so, which via layer

connects which pair of conductor layers? If we insert Fill in via layer, do we need to avoid the Fill in via layer touching the conductors in upper or lower layer?
A19. No via FILL. The test cases have been updated and all via layers have been removed.

Q20. In the testcases, there are via layers from layer 11~layer 19, but we don't have the corresponding capacitance table in process file. Is via involved in the capacitance calculation?
A20. Via layers have been removed.

Q21. In the testcases ,net 0 is set to both power net and ground net. Do we consider net 0 as ground net?
A21. Yes, this is made on purpose. All nets with ID 0 are ground nets.

Q22. We can't find the window size in process file.
A22. Please re-download the cases. It has been added into the process file.

Q23. Is there any hard limit on run time?
A23. Yes, 24 hours.

Q24. The question is about testcase file.
In “process.dat”, the amounts of unit capacitance at the first line of table are one more than second line of table.
For example, there are 12 range numbers at line 23, but 11 parameters of function. In cap extraction example, you give both of them a same amount. Therefore, if I got three values which was defined as “area_table_1_0”,
1600, 2400, 320000. And which parameters of function will be chosen, respectively?
A24. Yes, the examples in the problem description missed one sampling point. Thanks for pointing that out. Assuming a parameter x, and a series of sampling point x_1 x_2 x_3 .. x_n. If x_k =< x <x_k+1, you should choose the kth function coefficient. If x is out of the sample region, i.e., x < x_1 or x >= x_n, please see the problem description on how to scale or discard the values.

Q25. May I know in the contest question C, for the total capacitance, what is the exact way to calculate the total capacitance? in the example, there is only mention the capacitance between the critical and non-critical net, or should we just sum up all the capacitance in the final evaluation?
A25. To calculated the total cap:

1. "the total capacitance of a critical net will be calculated as the equivalent capacitance to ground"
2. Total cap = sum of the total capacitance of each critical net.
For step 1, it's a basic pure capacitor-network analysis that calculates the equivalent capacitance of a two-port cap-network.
If you don't know how to do this, please refer to
https://en.wikipedia.org/wiki/Series_and_parallel_circuits
https://en.wikipedia.org/wiki/Capacitor#Networks
slides 10-11
of http://www.ece.ubc.ca/~shahriar/eece251_notes/eece251_set4_2up.pdf
for the basic rules of capacitance calculation.

Q26. How do we read file path ? Is use absolute path or other path?
A26. Please use the path that is relative to the config file.

Q27.

Q1: As shown in Fig. 1, suppose nets A and B in layer 1 and layer 3, respectively. Meanwhile, their projections on the ground plane overlap. If a small net C in layer 2 cross the overlapping region of projection between nets A and B, is the area capacitance between nets A and B completely shielded by net C (i.e., $C_3^a = 0$)? If not, how to calculate C_3^a?

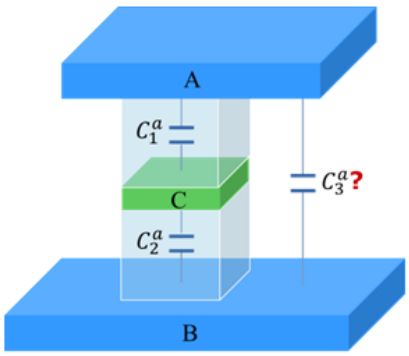


Fig. 1 Area capacitance

A27. No, C{^a}_{3} is not zero. The area cap is formed by the overlapped area in which two conductors that form this area can directly "see" each other.
In your case, A/C formed an area. Inside the area, A and C can directly "see" each other and its area cap would be calculated as C1. C/B formed an area
inside which B/C can see each other and its area cap would be calculated as C2. The other overlapped area, i.e., the area that A/B can directly "see"
each other would be calculated as C3.

Q28.

Q2: As shown in Fig. 2, suppose nets A, B and C belong to the same layer and net B is between nets A and C (Note: there are lateral capacitance between any two nets). In Fig. 2 (a), is the lateral capacitance between nets A and C shielded by net B? If there can be shield, then in Fig. (b), is the lateral capacitance between nets A and C completely shielded by net B (i.e., $C_3^l = 0$)? If $C_3^l \neq 0$, does the calculation of the lateral capacitance between nets A and C be affected by net B? If it does, what is the detailed calculation formula for the lateral capacitance C_3^l between nets A and C?

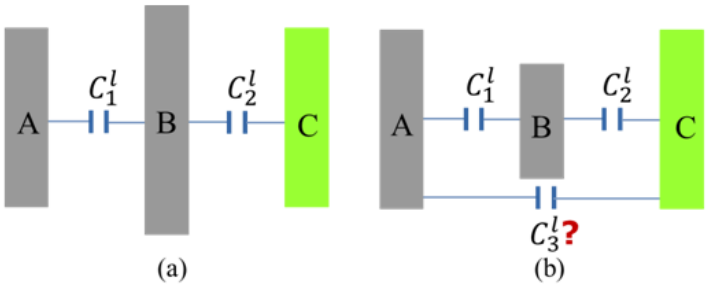


Fig.2 Lateral capacitance shielding. (a) Example 1. (b) Example 2.

A28. This is similar to Q1. If any part of A/C cannot see each other (horizontally), C3 is 0 (case a). If any part of A/C can "see" each other, that part should have lateral coupling cap.

The calculation is similar as the calculation of c1l or c2l. i.e., with the parallel edge of A/C and distance between A/C. Please note the parallel edge only contains the part in which A/C can directly see each other.

Here is how to calculate caps in b:

Assuming A&B's parallel edge is l_ab (which is actually B's length as B is within a's horizontal projection), and the distance between A&B is d_ab,

C1l = P(l_ab)*d_ab

Similar, we can cat C2l = P(l_bc)*d_bc.

Assuming A&C's parallel edge is l_ac, and the distance is d_ac, since part of A&C's parallel edge is blocked by B, then the effective parallel edge length should be

l_eff_ac = l_ac - l_ab (or l_ac - l_bc, since l_ab == l_bc),

C3l = P(l_eff_ac) * d_ac.

Q29. (You can check Q42. For more information.)

Q3: Suppose a structure with nets A, B, C in layer 1 and nets D, E in layer 2 (Notes: there is not fringe capacitance between nets C and D). The details are shown in following Fig. 3.

Case 1: Is the capacitance between net D and ground plane shielded by net B?

Case 2: There is a lateral capacitance between nets A and C, is it shielded by net B?

Case 3: If there is a fringe capacitance between nets A and E, is it shielded by nets B or D? If there can be shield, is also the fringe capacitance between nets B and E shielded by nets C or D?

Case 4: For the specific example shown in following Fig. 3, can you show me a whole formula for calculating the total capacitance of critical net A?

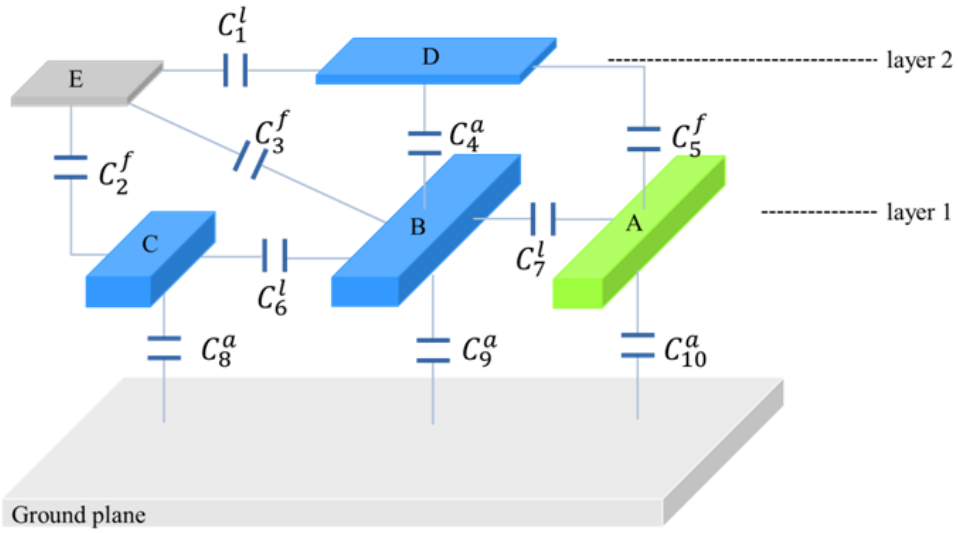


Fig.3 The total capacitance

A29.

Case 1: partly. Part of D may see the ground plane, so that part should have area cap to the ground. Please see A1 for more details.

Case2: It depends if A/C can directly see each other. Please see A2 for more information.

Case3: Fringe cap between A/E is shield by B/D/C. Fringe cap between B/E is also shielded (by D/C).

Case4: The case is too complicated to do a hand calculation. The standard method would be

doing a Y-delta transformation or using a matrix-based method (similar to conductance matrix based network analysis):

	A	B	C	D	E
A	(c5+c7+c10)	-c7	0	-c5	0

B -c7 (c3+c4+c6+c7+c9) -c6 -c4 -c3

C 0 -c6 .....

D -c5 -c4 .....

E 0 -c3 .....

Assuming the matrix is partitioned as follows:

C11 | C12

C21| C22

(C11 == (c5+c7+c10))
Then the total cap of A would be C11 - C12 * (1/C22)*C21

Q30. When calculating the area capacitance, you say "no other metal that appears on the layer between the two conductors crosses the overlapped region", thus, in the situation of figure a (please see figure a in the attachment), I think we do not need to calculate the area capacitance between layer1 and layer3. But how about the situations in figure b and figure c, can we still ignore the area capacitance between layer3 and layer1?

A30. For case a, since polygons on layer 3 and 1 are completely blocked by the red polygon, then there is no cap formed by the polygons on layer 3 and 1. If the polygons are not completely blocked by the red polygon, then the unblocked part of polygons on layer 1 and 3 will form area caps. In other words, if any two polygons on different layers, if they can vertically "see" each other, they form an area cap, the capacitance is determined by the size of the areas that they can "see" each other. So in case b and c, there are area capacitance between polygons on layer 1 and 3.

Q31. When calculating the fringe capacitance, as shown in figure d, we need to calculate the fringe capacitance between rect1 in layer1 and rect1 in layer2, do we still need to calculate the fringe capacitance between rect1 in layer1 and rect2 in layer2? If so, which part should be counted as the horizontally overlap between them?

A31. Yes. The similar rule of "being able to see each other" still applies to this case. For fringe cap between rect1 and rect2, the parallel edges that are not blocked by rect1 of layer 2 should be used to calculate fringe cap.

Q32. In the example of calculating the total capacitance, does C3 stands for the area capacitance between non-critical net A and non-critical net B or just the total equivalent capacitance between net A and net B? Should we calculate the fringe capacitance (C6) between critical net and non-critical net B?

A32. The example is only to show how to calculate the total cap. C3 is the area cap between net A and B. There should be fringe capacitance between B and the critical net.

Q33. Will the organizers release an official evaluation tool later?

A33. Yes, we are working on an evaluation tool and it's expected to be released around July.

"

Q34. Is min_width means both length and width of metal or each side of metal need to be larger than 65? (metal > 65x65)
Should the boundary conditions be set as > 65 or >= 65?

A34. Yes, the boundary conditions should be set as >=65.

Q35. For min_space, does it mean in the layer 1, the space between any two polygons should be > or >= 65?

A35. >=65

Q36. For max_fill width,
Should the boundary conditions be set as > 1300 or >= 1300?
Does this mean fill needs to be smaller than 1300 x 1300?

A36. <= 1300 and yes.

Q37. For fill and other polygons type, is min_space for each type of polygons all set as 65?

A37. Please refer to the rule files. The layer on which that the fills or polygons stay decides the min space.

Q38. For min_density and max_density for each layer, is that for one window? Is the density equals to (area of metal in the window / area of the window)?
A38. Yes and yes.

Q39. In the description of shielding effect you say "A and B is shielded when there is a horizontal conductor on the intermediate layer between A and B". But in A29 case3, you say "fringe cap between A/E is shield by B/D/C".
We note that E/D are on same layer, and A/B/C are one same layer, thus we want to confirm whether the "intermediate layer" includes layers that the target nets (e.g. A/E in A29 case3) lie in.
A39. Yes, the "intermediate layer" includes layers that the target nets (e.g. A/E in A29 case3) lie in.

Q40. We note that in the example conductance matrix of A29 case4, you also calculate the capacitances of each non-critical pair (e.g. c6 between non-critical net C and non-critical net B).
It would be very time/space consuming if we need to calculate capacitances of all net pairs (number of non-critical conductors is far more than number of critical conductors).
So we wonder if there is any method to approximate capacitances between non-critical net and non-critical net,
or if it is safe to ignore the capacitances between non-critical net and non-critical net?
A40. It's up to the contest participant to decide how to approximate the capacitance. This is the purpose of this contest, that is to find an efficient way to estimate the timing impact of the metal fills without heavy computational effort.

Q41. When you calculate the total cap of A (A29 case4), you partition the conductance matrix into C11, C12, C21, C22. Thus, for a nxn conductance matrix, C12 is a 1x(n-1) vector, C21 is a (n-1)x1 vector, and C22 is a (n-1)x(n-1) matrix, additionally, you calculate the inverse of a (n-1)x(n-1) matrix (e.g. 1/C22).
Our question is, how shall we partition the example matrix in A29 case4 if we want to calculate the total cap of net C? Or do we need to generate a new conductance matrix for calculating the total cap of net C, i.e. put net C in first col and first row of the matrix?

A41. Your understanding is correct. But A29 case4 is just an example to tell the participants that how we are going to evaluate the total cap. The participants don't have to follow the exactly same way.

Q42. In the response of Q29, says that we could use matrix-based method to calculate the capacitance of critical net A. And I am wondering how does this formula come out "Then the total cap of A would be C11 - C12 * (1/C22)*C21" ?

A42. Take the circuit in Q29 as an example:
Assuming we apply a current source i(t) into A and the potentials at A, B, C, D, E are Va(t), Vb(t), Vc(t), Vd(t), Ve(t) respectively, then for A, we can get
C10*Va' +C5*(Va - Vd)' + C7*(Va-Vb)' = i(t),
re-arranging the variables, we get:
(C10 + C5 +C7)va' - C7*Vb' - 0* Vc' -C5*Vd' - 0*Ve' = i(t)

For B, C, D, E, we can get similar equations:
B: -C7*Va' + (C7 + C6 + C4 + C3)*Vb' - C6*Vc' - C4*Vd' - C3*Ve' = 0
C: 0*Vc' - C6 + (C6+C2+C8) - 0*Vd' -C2V3' = 0
D: ...
E: ....

In matrix form:

| A | B | C | D | E | [v] [i]
---|---
A| C10 + C5 + C7 | -C7 | 0 | -C5 | 0 | | va'| |i(t)|
B| -C7 | C7+ C4 + C3 + C6 +C9| -C6 | -C4 | -C3 | | vb'| | 0 |
C| 0 | -C6 | C2+ C6 + C8 | 0 | -C2 | | vc'| = | 0 |
D| -C5 | -C4 | 0 | C5 + C4 + C1 | -C1 | | vd'| | 0 |
E| 0 | -C3 | -C2 | -C1 | C1 + C2 + C3 | | ve'| | 0 |

Now assuming the sub-matrix formed by column A and row A is C11,
C11 = [C10 + C5 + C7].
And assuming sub-matrix formed by row A and column B, C, D, E is C12,
C12 = [-C7 0 -C5 0].
Also assuming the sub-matrix formed by column A and row B, C, D, E is C21,
C21 = C12^T.
Assuming the sub-matrix formed by column B,C,D,E and row B, C,D, E is C22,
we can get a matrix form:
A11*Va' + A12 [Vb' Vc' Vd' Ve']^T = i(t) --------(1)
A21*Va' + A22[Vb' Vc' Vd' Ve']^T = [0] --------(2)

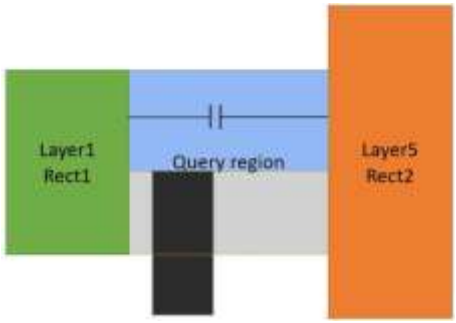
From (2) we can get
[Vb' Vc' Vd' Ve']^T = -[A22]^-1 * A21 * Va'
Then substituting the above vector into (1), we get
A11*Va' - A12*[A22}^-1*A21*Va' = i(t)
that is:
(A11 - A12*[A22]^-1*A21)*Va' = i(t)

The total equivalent cap between A and ground is
A11 - A12*[A22]^-1*A21

Q43. I want to ask if there is
an exist tool to check the capacitance of our output file?
A43. No there is no existing tool for the cap calculation.

Q44. For shielding effect:
"A and B is shielded when there is a horizontal conductor on the intermediate layer between A and B". We want to confirm what's meant by "between"? In our understanding, if we want to check whether there exists a shielding conductor "between" rect1 in layer1 and rect2 in layer5 (see in figure below), we will draw a smallest bounding rectangle (gray box in the figure) as the query box, and from layer1 to layer5, we will query if there is any rectangle intersecting with the query box. If so, rect1 and rect2 is shielded by that rectangle. Is our understanding correct?

A44. Your method is correct. But please be noted that if a rectangle only partly intersects with the query region, then the capacitance between Rect1 and Rect2 is only partly blocked and the unshielded fringe cap still needs be computed. Please see the picture for example.



Q45. Can we use multithread to execute our program? What are the limits and limitations of using multithread if we can apply this technique?

A45. You can use multi-threading, but we only provide one CPU core for each program (process).

Q46. In problem C, the first formula in page10 contains the value 0.0101 that doesn't exist in table area2_1.

A46. Thanks for pointing out this. There is a typo in table area_2_1. The value '0.00101' should be '0.0101'

Q47. Do we have to number the fill polygon from zero to the total number of the fill polygon?

Now assuming the metal-fill output file example1.fill:

```
1 30 0 40 80 0 2 Fill; A metal-fill on layer 2
```

A47. The first field is for polygon id. The 6th field is for net id. For fills, please set the 6th field to 0.

Q48.Does the given routing result on each layer with n conductors has any couplin g constraint? I don't see any coupling constraint in the .layout file, only the density constraint mentioned.

A48. No, there is no coupling constraint.

Q49. Can we use multithread to execute our program? And what the limitations of using multithread are if we can apply this technique?

A49. We don't impose threading limitation on the program. You can choose whatever programming techniques you like. But please note your program will be limited to one CPU core during its execution.

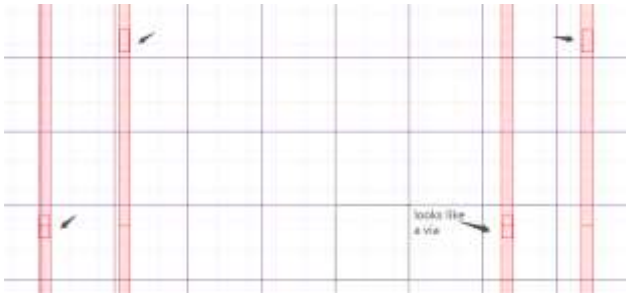
Q50. Can we insert dummy fill at the non-interger coodinates? For example, if the chip is bl (0,0) tr(1000,1000),is he dummy fill located at bl(0.5, 0.5) tr(100.5, 100.5) legal?

A50. No. All coordinates must be integer.

Q51. Is there be any tools that help us to check if our results not violate the design rule and the density requirement, and further to evaluate the performance of our results?

A51. We will release tools to check design rules and density violation in July.

Q52. We are working on dummy fill insertion problem, we find that in some windows of testcase2, the sum of fillable area and wire area is larger than the window area. After checking, we find that in *.cut file, some rectangles in same layer are overlap with each other, shown as below. All of these overlap rectangles are from P/G net (net 0), and they look like vias to connect the upper/lower layer. This kind of situation bring us some troubles to ensure correctness. So we wonder if it is necessary to keep these overlap rectanglesin same layer? If not, can you remove these rectangles from *.cut files?



A52. Thanks for pointing out this. These are via enclosures. We will remove them soon

Q53. when i star from one critical , others critical net are equal to ground or nothing and it still can be shielding effect ?

A: When you start from a critical net, other critical nets should not be treated as being grounded and should be treated as normal nets, meaning the coupling cap to those nets will be considered. And the shielding effect can still exist.

Q54. if there have many poly they are critical net and their critical net id is same , i need to do something special treatment to them ? or just treat them as different critical?

A: First of all, polygons with same net id belong to same net. You don't have to extract coupling cap between polygons of same net. Imagine a capacitor with two terminals being shorted together, it will not contribute effective capacitance to the signal net that it attaches to. In the final evaluation, the coupling cap between polygons of same net will be ignored.

Q55. In "rule." file,
the minimum width is 65, but the width of input metals is 63?

A56. The test data we released was cut out from real designs. We randomly added perturbation to the layouts.

Q56. For two neighbor fills,
the space between them should be larger than minimum space? or not?

A56. Must be larger (or equal) than min space.

Q57. Could contest committee please report the detailed test results (includes: total capacitance, the number of spacing violations, the number of density violations, etc) for each benchmark of alpha submission?

A57. If design rule checking is not passed, we will not do cap extraction.

Q58. According to A54 , Are
the normal polys that have same net_id considered as one point ? If problem's answer is yes , the every normal polys that have same net_id , it's capacitance value would need to add up?

A54. Yes.

Two cap values can be (and need be) added up as long as the nets they connect are same. For example, cap A connects to net 1 and net 2, cap B connects to net 1 and net 2, and cap C connects net 1 and net 3.

You can add up A and B, but C cannot be added up to A or B.

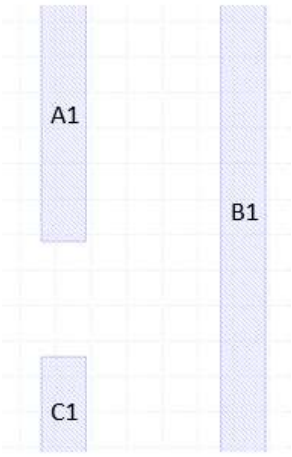
Q59. I have read the latest version of problem C FAQ, and I want to ask that is there a coupling capacitance between two "Fill" polygon?

A59. Yes.

Q60. In
the output file, do we need to output the original metal (polygons of nets) or we just only need to output the inserted dummy fills.

A60. Only fills.

Q61. We find that each layer have its own direction,
e.g. layer1 is horizontal and layer2 is vertical. And
the document says "any twoconductors that **horizontally overlap** will form lateral capacit ance". We want to figure out the exact meaning of "**horizontally overlap**". In our understanding, we will only calculate the lateral capacitance between rectangle pair whose overlap is on horizontal direction.
For example, rectangles A1, B1, C1 are all in layer1 (see in figure 1 below),
and we will only count the lateral cap between A1-B1 and C1-B1 (**horizontally overlap**), and there is no lateral cap between A1-C1.



Similarly, A2, B2, C2, D2 are all in layer2 (see in figure 2 below), and we will count the lateral cap between C2-D2 (**horizontallyoverlap**).

Thus, the lateral cap will be small for layer2. So we want to know do we need to change the "horizontal overlap" into "vertical overlap" for horizontal layer (like layer2)?
Or we need to consider both horizontal and vertical overlap for each layer?
Actually this similar situation exist in fringe cap calculation. The "fringe capacitance per unit length" is a function of **horizontal distance** *d*, does it means we only need to calculate the fringe capacitance formed by "horizontal overlap"?
A61. "Horizontal" here means both x/y directions. You can imagine the layout as a 3-D structure. "Horizontal" means polygons on the samelayer. "Vertical" means polygons on different layers. So in your examples, both need extract lateral caps.

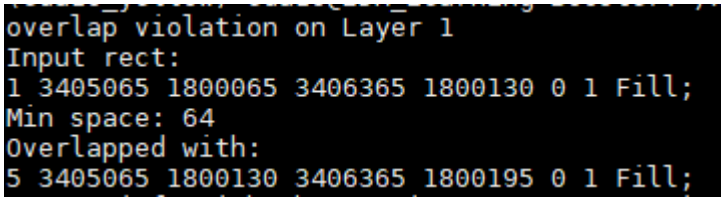
Q62. Our output do not pass the DRC in alpha submission, but we do not find any design rule violation through our DRC scripts.
The answer of Q51 says that an official tool of DRC will be released in July. The ddl of beta is coming soon, we want to get a score feedback through beta report. So would you please release the DRC tool so that we can find out our DR violations and submit a legal solution in BETA?
A62. The tool has been released. (The older version of the checker has a bug which may incorrectly reported the violations). Please use the latest version to check your design.

Q63. It seems that the via enclosures mentioned in Q52 haven't been removed yet, would you please help us to remove them?
A63. The new data has been released (via enclosure removed) today. Please download the circuit*.cut.tar.gz and replace the old cut files with the new files.

Q64. Should the output file include the original conductors?
Or just output the metal fills?
A64. Please output the fill into a separate file (the file name is specified inside .config file)

Q65. I found circuit3.cut also has some via enclosures, can you remove them?
A65. 1. The data with via enclosure being removed has been uploaded.
You may download the updated .cut file in circuit*.cut.tar.gz from
https://github.com/boyangeda/iccad2018-contest

Q66. Why two dummy fills connect each other have overlap(spacing) violation?



A66. Because the design rules we released for the contest are very basic rules, if we allow touch/overlap of fills, it would involve a very complicate rule database and the contestants would need commercial tool to check the layout.

Q67. We have finished the execution of capacitance extraction, and get an output file. The format of output file is <netid1> <netid2> <capvalue>, we want to know how to the get the objective value (total capacitance of a given critical nets) through the output file. Can we just sum up the <cap value> of critical nets? Or we need to calculate the equivalent capacitance of critical nets by ourselves and sum them up?

A67. We don't require the contestants providing the equivalent capacitance of the critical nets. We only need the fill file. The purpose of theextraction tool is to let the contestants to evaluate their own cap estimator if they want to, not to calculate the total cap. Please note we use equivalent capacitance of critical nets to do the final evaluation.

Q68. Is there a executive command line to run our program or we just note how to execute our program in readme file.

A68. Please provide a readme file to describe how to run your program.

Q69. We found the circuit.cut file still have some conductors which overlapped. Will they be revised recently?

A69. Please download the new cut files from https://github.com/boyangeda/iccad2018-contest. Please use the cut files inside circuit*.cut.tar.gz to replace the old files.

Q70. Does the new checker need a fill format or exe file ?

A70. Yes. It needs a fill file along with the layout (.cut), design rule file. Please run the checker without any arguments to see the usage.

Q71. Does the cap extraction tool provide multi-thread option?
The time for cap extraction (uncertainty = 0.1)
on single thread is measured by days(especially for large cases).

A71. The purpose of the cap extraction tool is to help contestants calibrate their cap estimators with smaller cases, but not to serve as a fully functional extractor.

Q72. I have a question in cap extraction example, why the largest sampling point in the area_2_1 is 400nm^2 instead of 500?

```
TableName: area_2_1
  100                 300          400       500
  (0.01, 0.017) (0.0102, -0.02) (0.00101, 0.015)
```

A72. hanks for point out it. This is a typo. The largest point should be 500.